IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Atty. Dkt. No: 5150-38605 §
§
§

Inventor(s): §
  Robert E. Dye, Darshan K. §
  Shah, Steven W. Rogers, §
  Gregory C. Richardson, and §
  Dean A. Luick §
Title: GRAPHICAL §
  PROGRAMMING §
  SYSTEM WITH BLOCK §
  DIAGRAM EXECUTION §
  AND DISTRIBUTED
  USER INTERFACE
  DISPLAY

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant requests consideration of ☒ the references listed on the attached Form PTO-1449 and/or ☐ the additional information identified below in paragraph 3. A copy of each of the references listed on the Form PTO-1449 were previously submitted to or cited by the U.S. Patent and Trademark Office in U.S. Application Serial No. 09/617,600, to which the captioned application is seeking priority under 35 U.S.C. §120.

1. This Information Disclosure Statement is submitted:

 a. ☒ within 3 months of the filing date of a national application other than a continued prosecution application under § 1.53(d);

  ☐ within 3 months of the date of entry of the national stage as set forth in § 1.491 in an International application;

  ☐ before the mailing date of a first Office Action on the merits; or

☐ before the mailing of a first Office Action after the filing of a request for continued examination under § 1.114.

b. ☐ after the events of above paragraph 1a and prior to the mailing date of a final Office Action or Notice of Allowance, and thus: ☐ the certification of paragraph 2 below is provided, or ☐ a fee of $180.00 is enclosed.

c. ☐ after the mailing date of a final Office Action or a Notice of Allowance and prior to payment of the issue fee, and thus: the certification of paragraph 2 below is provided and a fee of $180.00 is enclosed.

2. It is hereby certified:

☐ that each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the Statement, or

☐ that no item of information contained in the Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the person signing the certification after making reasonable inquiry, was known to any individual designated in § 1.56 (c) more than three months prior to the filing of the Statement.

3. ☐ Consideration of the following additional information (including any co-pending or abandoned U.S. applications, prior uses and/or sales, etc.) is requested:

4. For each non-English language reference listed on the attached Form PTO-1449:

☐ reference is made to an English language translation submitted herewith, and/or

☐ reference is made to a foreign patent office search report (in the English language) submitted herewith, and/or

☐ reference is made to an English language translation of a foreign patent office search report submitted herewith, and/or

☐ reference is made to the concise explanation contained in the specification of the present application at page(s)_____, and/or

☐ reference is made to the concise explanation set forth below:

5. ☐ Applicant also offers the following comments for the Examiner's consideration:

6. ☐ Also enclosed is a copy of a foreign search report citing these references.

7. ☐ The listed documents were brought to the attention of the Applicant(s) after payment of the issue fee in the captioned case. The documents were cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. Applicant(s) request this Information Disclosure Statement and attached Form PTO-1449 be placed in the file of the captioned application.

8. ☐ Applicant(s) request that the Information Disclosure Statement and attached Form PTO-1449 and references, which are being filed before the grant of the patent and pursuant to 37 C.F.R. § 1.97(i), be placed in the file of the captioned application.

CHANGE OF ADDRESS

The Patent Office is respectfully requested to direct all future correspondence for this case to the below-referenced address.

If any required fees are missing, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert & Goetzel PC Deposit Account No. 50-1505/5150-38605/JCH.

Respectfully submitted,

Jeffrey C. Hood
Reg. No. 35,198
Attorney for Applicant(s)

Meyertons, Hood, Kivlin, Kowert & Goetzel PC
P.O. Box 398
Austin, Texas 78767-0398
(512) 853-8800

Date: February 5, 2004

Form PTO-1449 (modified) List of Patents and Publications For Applicant's Information Disclosure Statement (Use several sheets if necessary)	ATTY. DOCKET NO: 5150-38605		SERIAL NO: Unknown
	APPLICANT: Dye et al.		
	FILING DATE: Herewith		GROUP: Unknown

FOREIGN PATENT DOCUMENTS

EXAM. INITIALS	REF. DES	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION. YES/NO
		WO 94 10627 A	5/11/94	PCT			
		WO 94 15311 A	7/7/94	PCT			

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

		De Coster, GRAPE-II: An Introduction [online]. Automatic Control and Computer Architectures Department. Katholieke Universiteit Leuven, Belgium, February 22, 1996 [retrieved October 6, 1999] Retrieved from the Internet @ http://www.esat.kuleuven.ac.be/acca
		Collamati et al. "Induction Machine stator Fault On-line Diagnosis Based on LabVIEW Environment", Mediterranean Electrotechnical Conference, Vol. 1, pg. 495-498, May 1996.
		Spoelder et al., "Virtual Instrumentation: A Survey of Standards and Their Interrelation", Proc. IEEE Instr. and Measurement Tech. Conf., Vol. 1, pp. 676-681, May 1997.
		Srinivasan et al., "LabVIEW program Design for On-Line Data Acquisition and Predictive Maintenance", Proc. Of the 30th Southeastern Symp. On System Theory, pp. 520-524, March 1998.
		Wahidanabanu et al., "Virtual Instrumentation with Graphical Programming for Enhanced Detection and Monitoring of Partial Discharges", Proc. Electrical Insulation Conf. 1997, pp. 291-296, September 1997.
	B1	Choosing Block-Diagram Tools for DSP Design, http://www.bdti.com/articles/info_dspmt95blockdiagram.htm, May 9, 2003, pgs. 1-7.
	B2	Real-Time Workshop for Use with Simulink, User's Guide, May 1994, 229 pages.
	B3	Guide to Rapid Prototyping with Simulink, Real-Time Workshop and dSPACE, 1995, 16 pages.
	B4	Real-Time Interface to Simulink, RTI 30, User's Guide, 1995, 125 pages.
	B5	Kevin J Gorman and Kourosh J. Rahnamai, "Real-Time Data Acquisition and Controls Using MatLAB", 1995, 4 pages.
	B6	SPW – MatLAB Co-Simulation Interface Product Data Sheet, 1996, 2 pages.
	B7	Signal Processing WorkSystem, MatLAB Interface User's Guide, Oct. 1995, 72 pages.
	B8	Alta Group of Cadence Design Systems, Inc., 1995, 34 pages.
	B9	Code Generation System Product Data Sheet, 1994, 8 pages.

Form **PTO-1449** (modified)	ATTY. DOCKET NO: 5150-38605		SERIAL NO: Unknown
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	APPLICANT: Dye et al.		
	FILING DATE: Herewith		GROUP: Unknown

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	B10	SPW/CGS Porting Kits Product Data Sheet, 11/94, 2 pages.
	B11	MultiProx for SPW Product Data Sheet, 08/94, 4 pages.
	B12	DSP ProCoder for SPW Product Data Sheet, 11/94, 4 pages.
	B13	Xanalog Corporation Sales Manual, January 1987, 8 pages.
	B14	Available XA-1000 Literature and Its Use, 1986, 2 pages.
	B15	Xanalog, XA-1000 Programming ICONS, 1986, 26 pages.
	B16	Xanalog's CAE System: The Fastest AT Alive, Mass High Tech, Vol. 4, No. 22, 08/1988, 1 page.
	B17	Xanalog The Computer Aided Engineering Workstation Comes to Simulation, Simulation Vol. 47, No. 1, July 1986, 3 pages.
	B18	Xanalog RT Real Time Analog and Digital I/O, 10/90, 4 pages.
	B19	Xanalog/SC+, 9/90, 4 pages.
	B20	Xanalog Specializing in Workstations for Continuous Dynamic Simulation, 1987, 24 pages.
	B21	Xanalog Real-Time User Guide, 1994, 28 pages.
	B22	Lee et al., "Gabriel: A Design Environment for Programmable DSPs", 11/7/1988, 13 pages.
	B23	Lee et al., "A Design Tool for Hardware and Software for Multiprocessor DSP Systems", May 1989, 4 pages.
	B24	Gabriel 0.7 Overview, 1990, 5 pages.
	B25	Joseph T. Buck and Edward A. Lee, "Scheduling Dynamic Dataflow Graphs with Bounded Memory Using the Token Flow Model", http://www.synopsys.com/, 1995, 4 pages.
	B26	Edward A. Lee, "Design Methodology for DSP", 1992, 4 pages.
	B27	Pino et al, "Interface Synthesis in Heterogeneous System-Level DSP Design Tools, 05/1996, 4 pages.
	B28	Jose Luis Pino, Master's Report, "Software Synthesis for Single-Processor DSP Systems Using Ptolemy", May 1993, 48 pages.
	B29	Asawaree Kalavade and Edward A. Lee, "A Hardware-Software Codesign Methodology for DSP Applications", 1993, 12 pages.
	B30	Pino et al., "Automatic Code Generation for Heterogeneous Multiprocessors", 1994, 4 pages.
	B31	Tool Chest continues to Grow, Electronic Engineering Times, 12/15/1995, 2 pages.
	B32	Pino et al., "Mapping Multiple Independent Syunchronous dataflow Graphs onto Heterogeneous Multiprocessors, 10/1994, 6 pages.
	B33	Asawaree Kalavade and Edward A. Lee, "Hardware/Software Co-Design Using Ptolemy – A Case Study, 09/1992, 18 pages.
	B34	Pino et al, "Software Synthesis for DSP Using Ptolemy", 1995, 15 pages.
	B35	Vol. 1 – Ptolemy 0.7 User's Manual, 1997, 532 pages.
	B36	i-Logix Product Overview, 1996, 52 pages.
	B37	Press Release, i-Logix Statemate MAGNUM Supports PCs", 01/31/1997, 2 pages.
	B38	Press Release, "i-Logix Signs Reseller Agreement for Virtual Prototypes, Inc.'s VAPS Product Line, 02/11/1997, 2 pages.
	B39	Press Release, "i-Logix Introduces Rhapsody, Object-Oriented analysis, Design and Implementation Tool", 02/10/1997, 2 pages.

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OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	B40	Statemate/C Product Overview, 1995, 4 pages.
	B41	Press Release, "i-Logix and Integrated Systems Link Statemate MAGNUM and MATRIX AutoCode" 01/03/1997, 2 pages
	B42	Press Release, "i-Logix and Wind River unveil Industry's First Rapid Prototyping Solution for Testing Embedded Systems at ESC West in San Jose, 09/17/1996, 3 pages.
	B43	Press Release, "i-Logix Inc. Endorses Unified Modeling Language, 01/16/1997, 1 page.
	D1	Philip Dean Lapsley, "Host Interface and Debugging of Dataflow DSP Systems", Thesis, 1991, pgs. 1-51.
	D2	Lee et al., "Gabriel: A Design Environment for Programmable DSPs", 1988, pgs. 1-11.
	D3	Lee et al., "Gabriel: A Design Environment for DSP", IEEE Transactions on Acoustics, Speech, and Signal Processing, Vol. 37, No. 11, Nov. 1989, pgs. 1751-1762.
	D4	Bier et al., "Gabriel: A Design Environment for DSP", IEEE Micro Issue – Vol. 10, No. 5, 1990, pgs. 28-45.
	U	Ludolph et al., "The Fabrik Programming Environment", IEEE, pages 222-230, 1988.

EXAMINER:	DATE CONSIDERED:

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the patent owner.